Homework Assignment #8
Due In Class Tuesday April 7th

1. Brown & Vranesic 7.1

2. Brown & Vranesic 7.3


5. Brown & Vranesic 7.16

6. Brown & Vranesic 7.17

7. Brown & Vranesic 7.18. Verify your answer using the Quartus simulator and turn in a printout of your schematic and waveform. T Flip-Flops can be found under the library Primitives→Storage→tff. Note, this T Flip Flop has low true preset and clear inputs that you can tie to a constant value (Primitives→other→vcc or gnd)

8. Brown & Vranesic 7.34

1. The figures below show a sequential logic device and a timing diagram. The signals X, Y and CLK shown in the timing diagram are applied to the inputs of the device, and you must complete the timing diagrams for the signals J, K and Q. You should assume that, as shown in the figure for $t < 0$, CLK = X = Y = Q = 0, and J = K = 1. Also note that the propagation delay for any component (typically on the order of ns) is much smaller than the period of the clock signal (4 ms).

![Timing Diagram](image-url)