Homework Problems: The following problems are to be completed and turned in by the beginning of class on the due date.

1. Read Brown & Vranesic Section 2.7 before attempting this problem! This problem is concerned with the use of the logical operations NAND and NOR, which are the complements of the AND and OR operations, respectively. That is,
\[ x \text{ NAND } y = \overline{x \cdot y} \]
\[ x \text{ NOR } y = \overline{x + y} \]
There are of course logic gates that implement these operations. The symbols for NAND and NOR gates are illustrated in Figures 2.6(a) and 2.6(b) of Brown & Vranesic.

(a) Demonstrate that the following Boolean equation is true by using algebraic manipulation.
\[ ab + cd = \overline{a \cdot b \cdot c \cdot d} \]

(b) Draw two functionally equivalent logic networks that represent each side of the above equation. The network for the left side should be in sum-of-products form, and the network for the right side should use only NAND gates.

(c) What significance do the results of parts (a) and (b) have for the implementation of sum-of-products logic networks?

(d) Demonstrate that the following Boolean equation is true by using algebraic manipulation.
\[ (a + b)(c + d) = \overline{a + b + c + d} \]

(e) Draw two functionally equivalent logic networks that represent each side of the above equation. The network for the left side should be in product-of-sums form, and the network for the right side should use only NOR gates.

(f) What significance do the results of parts (d) and (e) have for the implementation of product-of-sums logic networks?

2. Brown & Vranesic 3.5.
6. Determine the Boolean function for OUT, as implemented by the following static CMOS circuit.
6. This problem requires you to evaluate and extend some of the results from Homework Assignment 2, Problem 7, which itself was an extension of B&V Problem 2.36. Make sure you fully understand the posted solution to HW2 P7 before attempting this problem.

(a) Consider the minimal SOP network shown in part (d) of the solution. Suppose that this network were implemented using the standard CMOS circuit for each logic gate. How many transistors would be required?

(b) Redraw the SOP network so that it uses only NAND gates. If this network were implemented, using the standard CMOS circuit for each NAND gate, how many transistors would be required?

(c) Next, consider the minimal POS network shown in part (f) of the solution. Suppose that this network were implemented using the standard CMOS circuit for each logic gate. How many transistors would be required?

(d) Redraw the POS network so that it uses only NOR gates. If this network were implemented, using the standard CMOS circuit for each NOR gate, how many transistors would be required?

(e) Design a CMOS complex gate that implements the desired function. Your solution must use as few transistors as possible. There are two solutions that use the same number of transistors. Show your derivations, and draw a schematic for each circuit.

Recitation Problems: The following problems are not to be turned in. Instead, the solutions to these problems will be presented at the recitations. You should try these problems on your own before coming to recitation.

2. Brown & Vranesic 3.4