Implementation Technologies: Transmission Gates and Buffers and Programmable Logic
Transmission Gates

(a) Circuit

(b) Truth table

(c) Equivalent circuit

(d) Graphical symbol
Exclusive-OR Gates

<table>
<thead>
<tr>
<th>$x_1$</th>
<th>$x_2$</th>
<th>$f = x_1 \oplus x_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<td>1</td>
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<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

(a) Truth table

(b) Graphical symbol

(c) Sum-of-products implementation
Transmission Gate Exclusive-OR

\[ x_1 \]
\[ x_2 \]

\[ f \]
2-to-1 Multiplexers (2:1 Mux)

- Multiplexer circuits are used to forward one of multiple inputs, to a single output
2-to-1 Multiplexer Implementations

• In many cases, we can significantly reduce the cost of the circuit, just by changing the implementation technology
Buffer Circuits

- **Buffers** are logic gates with one input and one output and the logical value of the output is the same as the input.

- Buffers are not useful from a logic perspective. However, they are widely used for electrical reasons (e.g. improving signal quality).
Tri-State Buffers

- **Tri-State Buffers** are buffers that can output one of three possible states (0, 1, Z)
Tri-State Buffer Implementation

Implementation

Truth Table

<table>
<thead>
<tr>
<th>e</th>
<th>x</th>
<th>f</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
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<td>0</td>
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<tr>
<td>1</td>
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</tbody>
</table>
Standard Chips

• In 1980s, common practice was to connect together multiple chips, each containing only a few logic gates

(a) Dual-inline package 7400-Series Chip
(b) Structure of 7404 chip
74HC00 Datasheet Handout
Implementing Logic Using 7400-series Chips
What Happens When Design Becomes Complex?

Standard Chip Implementation of a Microprocessor
Programmable Logic Devices

Programmable logic device as a black box

- PLDs contain large amounts of logic circuit elements that can be customized in different ways
- There are many different types of PLD structures
Programmable Logic Array (PLA)

- PLAs are programmable devices for implementing SOP forms
  - **Input Inverters / Buffers:** Complement / Pass Inputs

- **AND Plane:** Form Product Terms
- **OR Plane:** Form Sums

General Structure of a PLA
Programmable Logic Array (PLA)

- Entire network is included on a single chip

- There is some programmable method by which the connections to the AND /OR gates can be established
Configuring Programmable Devices

- Connections are specified via CAD software
- High voltage “fuses” are used to make connections
Programmable Logic Array (PLA)

- Drawing out all possible connections awkward for larger chips
- Inputs drawn as a single line. Connections of an output to the input of a gate are denoted by X
- Useful for generating SOP functions that share common product terms
Programmable Array Logic (PAL)

- Difficulty in reliably manufacturing PLAs led to the development of a similar device, PALs.
- PALs have a programmable AND plane, but a fixed OR plane.
- Tradeoff in reliability is less flexibility; thus, they are manufactured in a wide range of sizes.

Symbolic Representation of a Programmed PAL
Programmable Array Logic (PAL)

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Extra circuitry added to output of PAL OR gates

Extra interface circuitry, called Macrocells, are added to each output:

- Tri-state buffer enables/disables the output
- A “Flip-Flop” is used to store the output
- A mux is selects which output drives the tri-state buffer
- Outputs are fed-back so that multi-level logic can be implemented
PAL22V10 Datasheet Handout
Complex Programmable Logic Devices (CPLDs)

- PALs are useful for small circuits, but are limited by number of inputs/outputs
- CPLDs are comprised of multiple PAL-like devices on a single chip, connected by IO blocks